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5. ~~(New) The integrated circuit of claim 4 further comprising~~ a substrate connected to the first through four surface structures, the inner plug, ~~and the first and second outer plugs~~.

4. ~~6.~~ (New) The integrated circuit of claim ~~5~~ 3, wherein the first through four surface structures are spaced apart along the substrate.

5. ~~7.~~ (New) The integrated circuit of claim ~~4~~ 2 further comprising a first outer contact region connected to the first outer plug.

6. ~~8.~~ (New) The integrated circuit of claim ~~7~~ 5, wherein the first contact region is tapered.

7. ~~9.~~ (New) The integrated circuit of claim ~~8~~ 6 further comprising a second outer contact region connected to the second outer plug.

8. ~~10.~~ (New) The integrated circuit of claim ~~4~~ 2, wherein the first and second outer plugs are on opposing sides of the inner plug.

9. ~~11.~~ (New) The integrated circuit of claim ~~10~~ 8, wherein the first and second spacers are located on opposing sides of the inner plug.

12. (New) An integrated circuit comprising:

a substrate having a plurality of source/drain regions;

a first, a second, a third, and a fourth surface structure located on the substrate, each having a top surface;

an inner plug connected to one of the source/drain regions, the inner plug being located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

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a first outer plug connected to one of the source/drain regions, the first outer plug having an upper portion covered the top surface of each of the first and third surface structures, and a

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second outer plug connected to one of the source/drain regions, the second outer plug having an upper portion covered the top surface of each of the second and four surface structures;

an inner electrical contact connected to the inner plug;

a first spacer for separating the inner plug and the inner electrical contact from the first outer plug, and a second spacer for separating the inner plug and the inner electrical contact from the second outer plug;

an isolation for covering the inner electrical contact; and

an outer contact region connected to the first outer plug.

13. (New) The integrated circuit of claim 12 further comprising another outer contact region connected to the second outer plug.

14. (New) The integrated circuit of claim 12, wherein the first and second outer plugs are on opposing sides of the inner plug.

15. (New) The integrated circuit of 12, wherein the first and second spacers are located on opposing sides of the inner plug.

16. (New) An integrated circuit comprising:

a substrate having a plurality of source/drain regions;

first and second insulated wordlines located on the substrate, each having a top surface;

a bitline plug connected to one of the source/drain regions, the bitline plug being located in between the first and second insulated wordlines and beneath the top surface of each of the first and second insulated wordlines;

a pair of storage node plugs, each being connected to one of the source/drain regions, each of the storage node plugs having an upper portion covered a portion of the top surface of one of the first and second insulated wordlines;

a bitline connected to the bitline plug; and

a pair of spacers for separating the bitline plug and the bitline from the pair of storage node plugs.

17. (New) The integrated circuit of claim 16 further comprising a first storage node connected to one of the storage node plugs.

18. (New) The integrated circuit of claim 17 further comprising a second storage node connected to the other storage node plug.

19. (New) The integrated circuit of claim 16, wherein storage node plugs are on opposing sides of the bitline plug.

20. (New) The integrated circuit of claim 16, wherein the pair of spacers are located on opposing sides of the bitline plug.

21. (New) An integrated circuit comprising:

a control unit; and

a storage unit connected to the control unit, the storage unit including:

a first, a second, a third, and a fourth surface structure, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a first outer plug having an upper portion covered the top surface of each of the first and third surface structures, and a second outer plug having an upper portion covered the top surface of each of the second and four surface structures;

an inner electrical contact connected to the inner plug;

a first spacer for separating the inner plug and the inner electrical contact from the first outer plug, and a second spacer for separating the inner plug and the inner electrical contact from the second outer plug; and

an isolation for covering the inner electrical contact.

22. (New) The integrated circuit of claim 21 further comprising a first outer contact region connected to the first outer plug.

23. (New) The integrated circuit of claim 22, wherein the first contact region is tapered.

24. (New) The integrated circuit of claim 23 further comprising a second outer contact region connected to the second outer plug.

25. (New) The integrated circuit of claim 21, wherein the first and second outer plugs are on opposing sides of the inner plug.

26. (New) The integrated circuit of claim 25, wherein the first and second spacers are located on opposing sides of the inner plug.

27. (New) An integrated circuit comprising:

a control unit; and

a storage unit connected to the control unit, the storage unit including:

a substrate having a plurality of source/drain regions;

first and second insulated wordlines located on the substrate, each having a top surface;

a bitline plug connected to one of the source/drain regions, the bitline plug being located in between the first and second insulated wordlines and beneath the top surface of each of the first and second insulated wordlines;

a pair of storage node plugs, each being connected to one of the source/drain regions, each of the storage node plugs having an upper portion covered a portion of the top surface of one of the first and second insulated wordlines;

a bitline connected to the bitline plug; and

a pair of spacers for separating the bitline plug and the bitline from the pair of storage node plugs.

28. (New) The integrated circuit of claim 27 further comprising a first storage node connected to one of the storage node plugs.

29. (New) The integrated circuit of claim 28 further comprising a second storage node connected to the other storage node plug.

30. (New) The integrated circuit of claim 27, wherein storage node plugs are on opposing sides of the bitline plug.

31. (New) The integrated circuit of claim 27, wherein the pair of spacers are located on opposing sides of the bitline plug.

Claims 2-3 are canceled and claims 4-31 are added. Claims 1 and 4-31 are now pending in this application. The Examiner is invited to contact Applicant's Representative (612) 373-6969 with any questions regarding the present application.

Respectfully submitted,

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Name Amy Moriarty Signature _____